

# TOSHIBA TC551001CP/CF/CFT/CTR/CST/CSR-55,-70,-85,-55L,-70L,-85L

TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

131,072-WORD BY 8-BIT STATIC RAM

## DESCRIPTION

The TC551001CP/CF/CFT/CTR/CST/CSR is a 1,048,576-bit static random access memory (SRAM) organized as 131,072 words by 8 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 5 V  $\pm$  10% power supply. Advanced circuit technology provides both high speed and low power at an operating current of 5 mA/MHz (typ) and a minimum cycle time of 55 ns. It is automatically placed in low-power mode at 1  $\mu$ A standby current (typ) when chip enable ( $\overline{CE1}$ ) is asserted high or ( $\overline{CE2}$ ) is asserted low. There are three control inputs.  $\overline{CE1}$  and  $\overline{CE2}$  are used to select the device and for data retention control, and output enable ( $\overline{OE}$ ) provides fast memory access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. The TC551001CP/CF/CFT/CTR/CST/CSR is available in a standard plastic 32-pin dual-in-line package (DIP), plastic 32-pin small-outline package (SOP) and normal and reverse pinout plastic 32-pin thin-small-outline package (TSOP).

## FEATURES

- Low-power dissipation  
Operating: 27.5 mW/MHz (typical)
- Single power supply voltage of 5 V  $\pm$  10%
- Power down features using  $\overline{CE1}$  and  $\overline{CE2}$ .
- Data retention supply voltage of 2 to 5.5 V
- Direct TTL compatibility for all inputs and outputs
- Standby Current (maximum) :

	TC551001CP/CF/CFT/CTR/CST/CSR	
	-55, -70, -85	-55L, -70L, -85L
5.5V	100 $\mu$ A	20 $\mu$ A
3.0V	50 $\mu$ A	10 $\mu$ A

- Access Times (maximum):

	TC551001CP/CF/CFT/CTR/CST/CSR		
	-55, -55L	-70, -70L	-85, -85L
Access Time	55 ns	70 ns	85 ns
$\overline{CE1}$ Access Time	55 ns	70 ns	85 ns
$\overline{CE2}$ Access Time	55 ns	70 ns	85 ns
$\overline{OE}$ Access Time	30 ns	35 ns	45 ns

- Packages:

DIP32-P-600-2.54 (CP)	(Weight: 4.45 g typ)
SOP32-P-525-1.27 (CF)	(Weight: 1.04 g typ)
TSOP I 32-P-0820-0.50 (CFT)	(Weight: 0.34 g typ)
TSOP I 32-P-0820-0.50A (CTR)	(Weight: 0.34 g typ)
TSOP I 32-P-0.50 (CST)	(Weight: 0.24 g typ)
TSOP I 32-P-0.50A (CSR)	(Weight: 0.24 g typ)

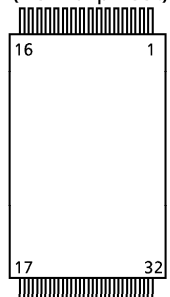
## PIN ASSIGNMENT (TOP VIEW)

### ○ 32 PIN DIP & SOP

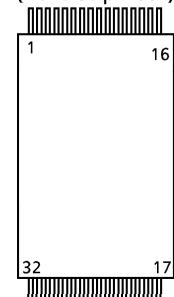
NC	1	32	V <sub>DD</sub>
A16	2	31	A15
A14	3	30	CE2
A12	4	29	R/W
A7	5	28	A13
A6	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	OE
A2	10	23	A10
A1	11	22	CE1
A0	12	21	I/O8
I/O1	13	20	I/O7
I/O2	14	19	I/O6
I/O3	15	18	I/O5
GND	16	17	I/O4

### ○ 32 PIN TSOP

(Normal pinout)



(Reverse pinout)



## PIN NAMES

A0 to A16	Address Inputs
R/W	Read/Write Control
OE	Output Enable
CE1, CE2	Chip Enable
I/O1 to I/O8	Data Input/Output
V <sub>DD</sub>	Power (+ 5 V)
GND	Ground
NC	No Connection

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pin Name	A <sub>11</sub>	A <sub>9</sub>	A <sub>8</sub>	A <sub>13</sub>	R/W	CE2	A <sub>15</sub>	V <sub>DD</sub>	NC	A <sub>16</sub>	A <sub>14</sub>	A <sub>12</sub>	A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>
Pin No.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Pin Name	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	CE1	A <sub>10</sub>	OE

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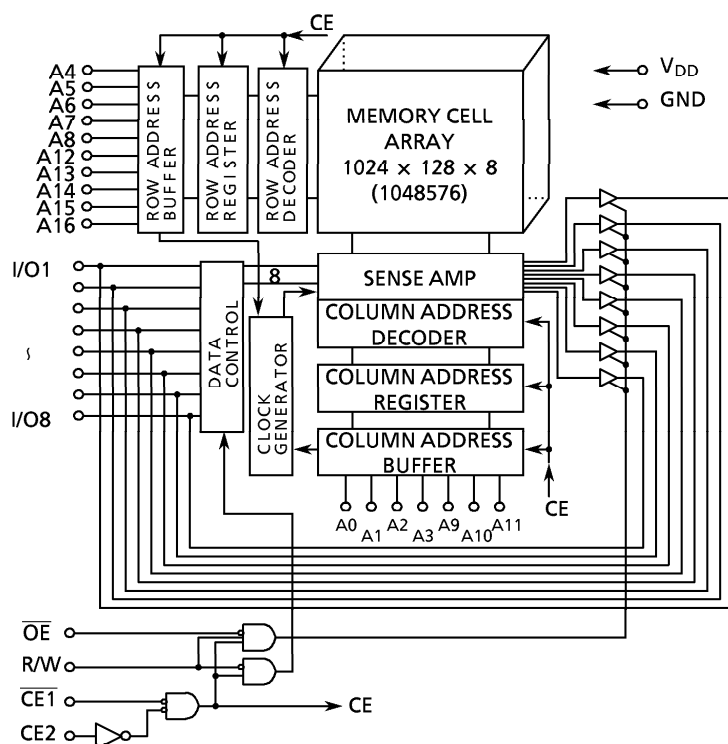
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# TOSHIBA TC551001CP/CF/CFT/CTR/CST/CSR-55,-70,-85,-55L,-70L,-85L

## BLOCK DIAGRAM



## OPERATION MODE

MODE	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	I/O1 to I/O8	POWER
Read	L	H	L	H	D <sub>OUT</sub>	I <sub>DDO</sub>
Write	L	H	x	L	D <sub>IN</sub>	I <sub>DDO</sub>
Outputs Disabled	L	H	H	H	High-Z	I <sub>DDO</sub>
Standby	H	x	x	x	High-Z	I <sub>DDS</sub>
	x	L	x	x	High-Z	I <sub>DDS</sub>

Note: x = don't care. H = logic high. L = logic low.

## ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V <sub>DD</sub>	Power Supply Voltage	- 0.3 to 7.0	V
V <sub>IN</sub>	Input Voltage	- 0.3* to 7.0	V
V <sub>I/O</sub>	Input and Output Voltage	- 0.5 to V <sub>DD</sub> + 0.5	V
P <sub>D</sub>	Power Dissipation	1.0/0.6**	W
T <sub>solder</sub>	Soldering Temperature (10 s)	260	°C
T <sub>strg.</sub>	Storage Temperature	- 55 to 150	°C
T <sub>opr.</sub>	Operating Temperature	0 to 70	°C

\* - 3.0 V when measured at a pulse width of 50 ns

\*\* SOP

# TOSHIBA TC551001CP/CF/CFT/CTR/CST/CSR-55,-70,-85,-55L,-70L,-85L

## DC RECOMMENDED OPERATING CONDITIONS (Ta = 0° to 70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.2	-	V <sub>DD</sub> + 0.3	
V <sub>IL</sub>	Input Low Voltage	- 0.3*	-	0.8	
V <sub>DH</sub>	Data Retention Supply Voltage	2.0	-	5.5	

\* - 3.0 V when measured at a pulse width of 50 ns

## DC CHARACTERISTICS (Ta = 0° to 70°C, V<sub>DD</sub> = 5 V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT													
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> = 0 V to V <sub>DD</sub>	-	-	± 1.0	μA													
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = 2.4 V	1.0	-	-	mA													
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.4 V	4.0	-	-	mA													
I <sub>LO</sub>	Output Leakage Current	$\overline{CE1} = V_{IH}$ or CE2 = V <sub>IL</sub> or R/W = V <sub>IL</sub> or $\overline{OE} = V_{IH}$ , V <sub>OUT</sub> = 0 V to V <sub>DD</sub>	-	-	± 1.0	μA													
I <sub>DDO1</sub>	Operating Current	CE1 = V <sub>IL</sub> and CE2 = V <sub>IH</sub> and R/W = V <sub>IH</sub> , I <sub>OUT</sub> = 0 mA Other Inputs = V <sub>IH</sub> /V <sub>IL</sub>	Tcycle = min	-55, -55L	-	-	80	mA											
				-70, -70L, -85, -85L	-	-	70												
			Tcycle = 1 μs		-	-	20												
I <sub>DDO2</sub>	Operating Current	CE1 = 0.2 V and CE2 = V <sub>DD</sub> - 0.2 V R/W = V <sub>DD</sub> - 0.2 V, I <sub>OUT</sub> = 0 mA Other Inputs = V <sub>DD</sub> - 0.2 V/0.2 V	Tcycle = min	-55, -55L	-	-	70	mA											
				-70, -70L, -85, -85L	-	-	60												
			Tcycle = 1 μs		-	-	10												
I <sub>DDS1</sub>	Standby Current	$\overline{CE1} = V_{IH}$ or CE2 = V <sub>IL</sub>  $\overline{CE1} = V_{DD} - 0.2 V$ or CE2 = 0.2 V V <sub>DD</sub> = 2.0 to 5.5 V					3	mA											
I <sub>DDS2</sub> (Note)														μA					
															-55, -70, -85	Ta = 25°C	-	1	-
																Ta = 0° to 70°C	-	-	100
	-55L, -70L, -85L	Ta = 25°C	-	1	2														
Ta = 0° to 70°C		-	-	20															

Note: In standby mode with  $\overline{CE1} \geq V_{DD} - 0.2 V$ , these limits are assured for the condition CE2  $\geq V_{DD} - 0.2 V$  or CE2  $\leq 0.2 V$ .

## CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = GND	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = GND	10	

Note: This parameter is periodically sampled and is not 100% tested.

# TOSHIBA TC551001CP/CF/CFT/CTR/CST/CSR-55,-70,-85,-55L,-70L,-85L

## AC CHARACTERISTICS AND OPERATING CONDITIONS ( $T_a = 0^\circ$ to $70^\circ\text{C}$ , $V_{DD} = 5\text{ V} \pm 10\%$ )

### READ CYCLE

SYMBOL	PARAMETER	TC551001CP/CF/CFT/CTR/CST/CSR						UNIT
		-55, -55L		-70, -70L		-85, -85L		
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{RC}$	Read Cycle Time	55	–	70	–	85	–	ns
$t_{ACC}$	Address Access Time	–	55	–	70	–	85	
$t_{CO1}$	Chip Enable ( $\overline{CE1}$ ) Access Time	–	55	–	70	–	85	
$t_{CO2}$	Chip Enable ( $CE2$ ) Access Time	–	55	–	70	–	85	
$t_{OE}$	Output Enable Access Time	–	30	–	35	–	45	
$t_{COE}$	Chip Enable Low to Output Active	10	–	10	–	10	–	
$t_{OEE}$	Output Enable Low to Output Active	5	–	5	–	5	–	
$t_{OD}$	Chip Enable High to Output High-Z	–	20	–	25	–	30	
$t_{ODO}$	Output Enable High to Output High-Z	–	20	–	25	–	30	
$t_{OH}$	Output Data Hold Time	10	–	10	–	10	–	

### WRITE CYCLE

SYMBOL	PARAMETER	TC551001CP/CF/CFT/CTR/CST/CSR						UNIT
		-55, -55L		-70, -70L		-85, -85L		
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{WC}$	Write Cycle Time	55	–	70	–	85	–	ns
$t_{WP}$	Write Pulse Width	45	–	50	–	60	–	
$t_{CW}$	Chip Enable to End of Write	5	–	60	–	75	–	
$t_{AS}$	Address Setup Time	0	–	0	–	0	–	
$t_{WR}$	Write Recovery Time	0	–	0	–	0	–	
$t_{ODW}$	R/W Low to Output High-Z	–	20	–	25	–	30	
$t_{OEW}$	R/W High to Output Active	5	–	5	–	5	–	
$t_{DS}$	Data Setup Time	25	–	30	–	35	–	
$t_{DH}$	Data Hold Time	0	–	0	–	0	–	

### AC TEST CONDITIONS

Output load: 30 pF + one TTL gate (-55, -55L)

: 100 pF + one TTL gate (-70, -70L, -85, -85L)

Input pulse level: 0.6 V, 2.4 V

Timing measurements: 1.5 V

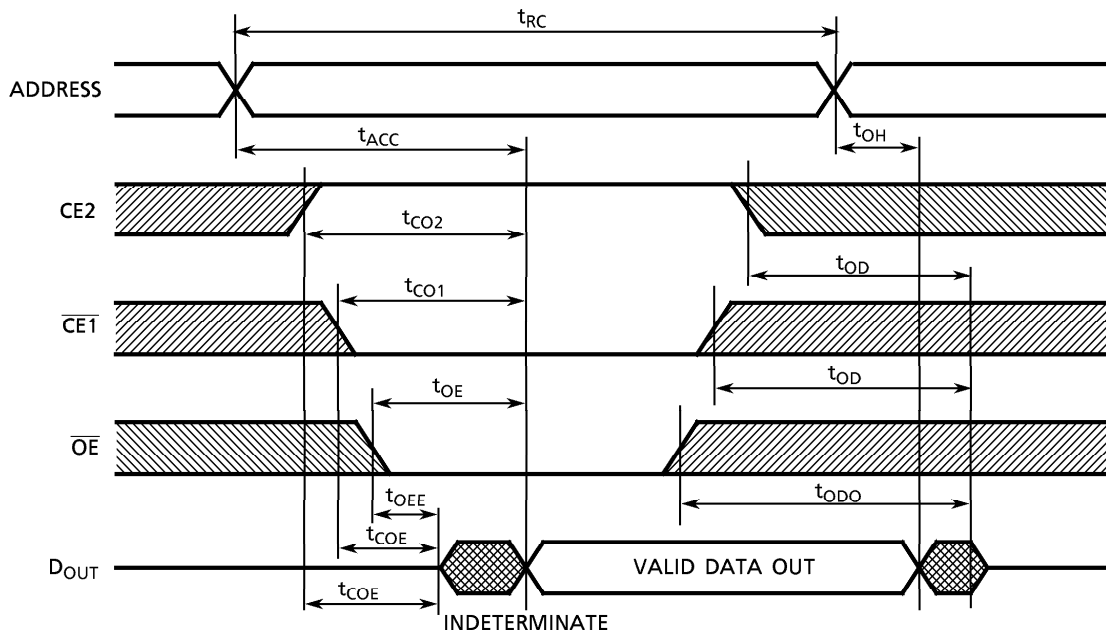
Reference level: 1.5 V

$t_R, t_F$ : 5 ns

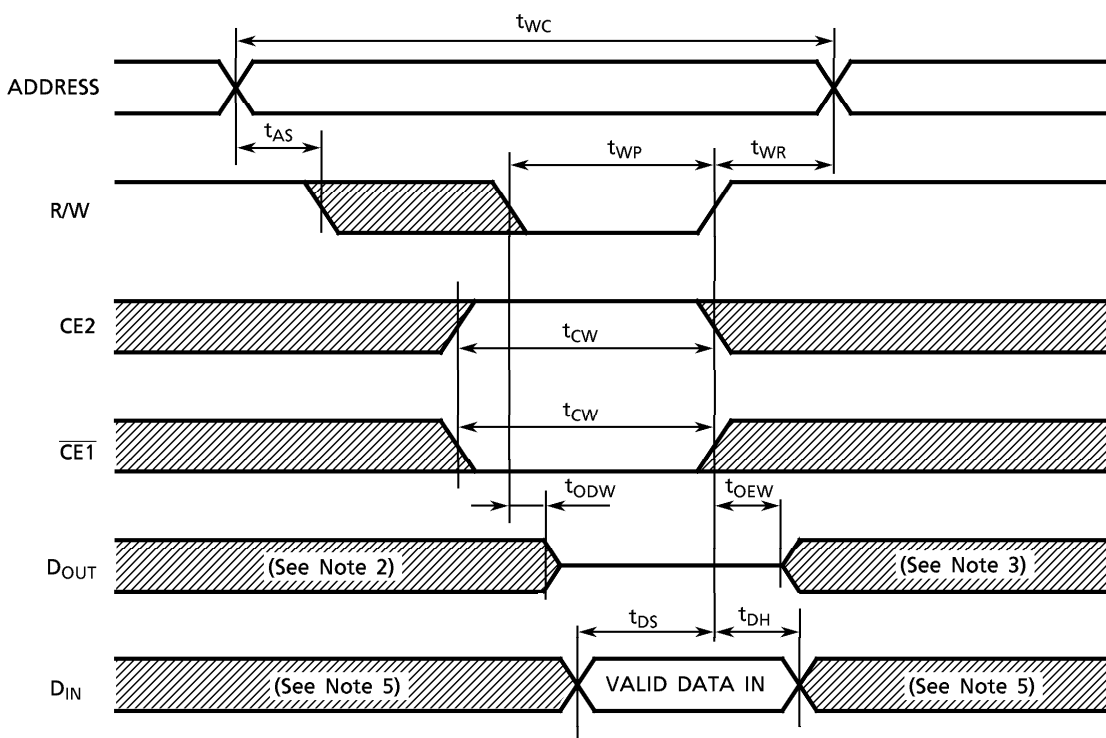
# TOSHIBA TC551001CP/CF/CFT/CTR/CST/CSR-55,-70,-85,-55L,-70L,-85L

## TIMING DIAGRAMS

### READ CYCLE (See Note 1)

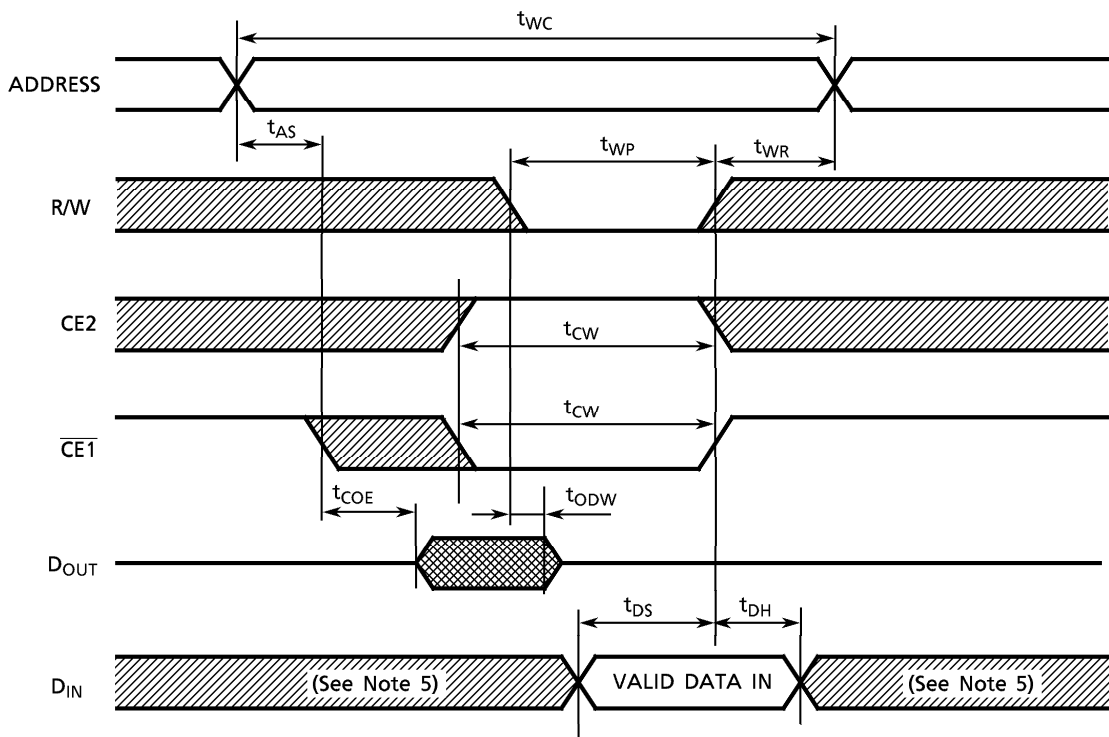


### WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)

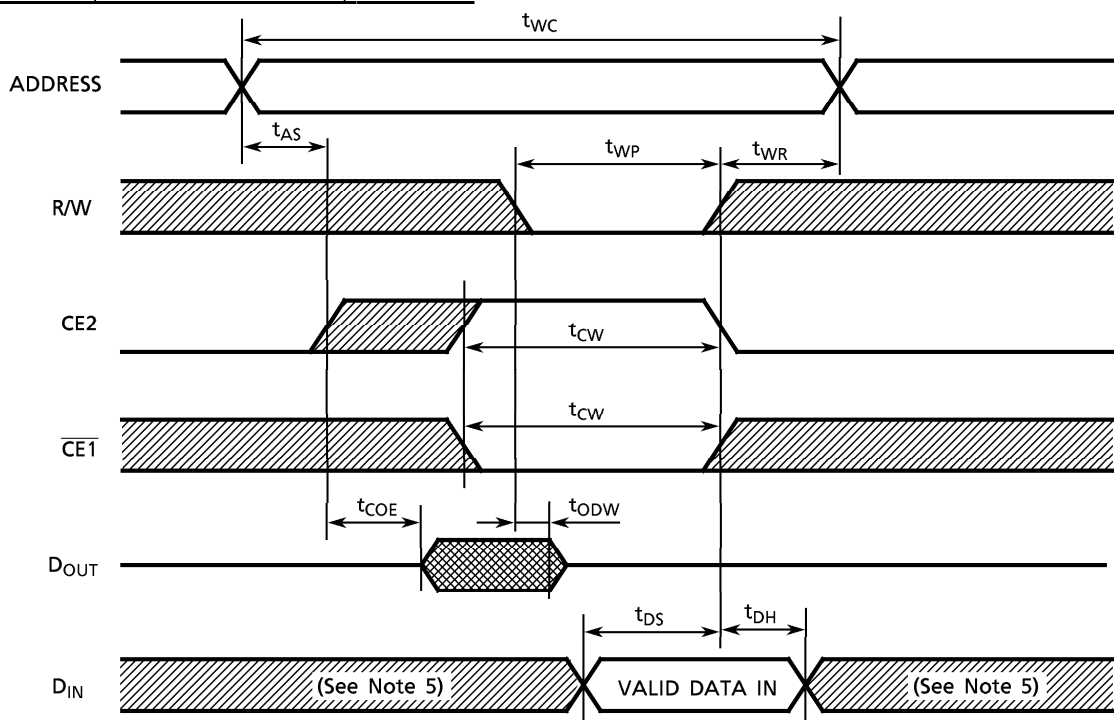


# TOSHIBA TC551001CP/CF/CFT/CTR/CST/CSR-55,-70,-85,-55L,-70L,-85L

## WRITE CYCLE 2 ( $\overline{CE1}$ CONTROLLED) (See Note 4)



## WRITE CYCLE 3 ( $\overline{CE2}$ CONTROLLED) (See Note 4)



# TOSHIBA TC551001CP/CF/CFT/CTR/CST/CSR-55,-70,-85,-55L,-70L,-85L

Note: (1) R/W remains HIGH for the read cycle.

(2) If  $\overline{CE1}$  goes LOW (or CE2 goes HIGH) coincident with or after R/W goes LOW, the outputs will remain at high impedance.

(3) If  $\overline{CE1}$  goes HIGH (or CE2 goes LOW) coincident with or before R/W goes HIGH, the outputs will remain at high impedance.

(4) If  $\overline{OE}$  is HIGH during the write cycle, the outputs will remain at high impedance.

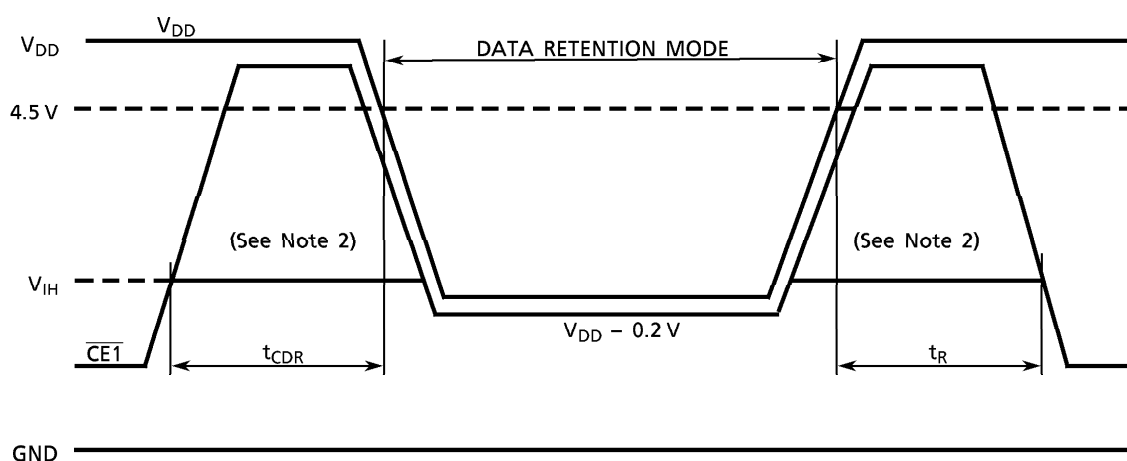
(5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

## DATA RETENTION CHARACTERISTICS (Ta = 0° to 70°C)

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT	
V <sub>DH</sub>	Data Retention Supply Voltage		2.0	–	5.5	V	
I <sub>DD52</sub>	Standby Current	-55, -70, -85	V <sub>DH</sub> = 3.0 V	–	–	50	μA
			V <sub>DH</sub> = 5.5 V	–	–	100	
		-55L, -70L, -85L	V <sub>DH</sub> = 3.0 V	–	–	10*	
			V <sub>DH</sub> = 5.5 V	–	–	20	
t <sub>CDR</sub>	Chip Deselect to Data Retention Mode Time		0	–	–	nS	
t <sub>R</sub>	Recovery Time		5	–	–	mS	

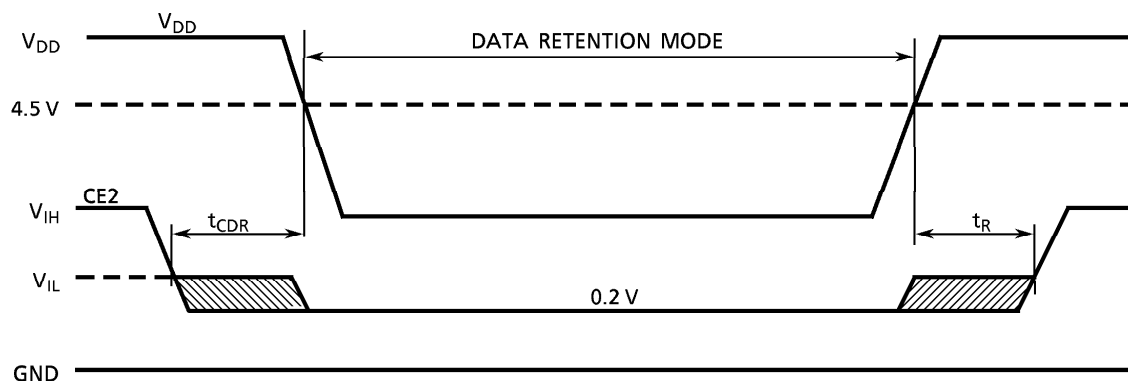
\* 2 μA (max) at Ta = 0° to 40°C

## CE1 CONTROLLED DATA RETENTION MODE (See Note 1)



# TOSHIBA TC551001CP/CF/CFT/CTR/CST/CSR-55,-70,-85,-55L,-70L,-85L

## CE2 CONTROLLED DATA RETENTION MODE (See Note 3)

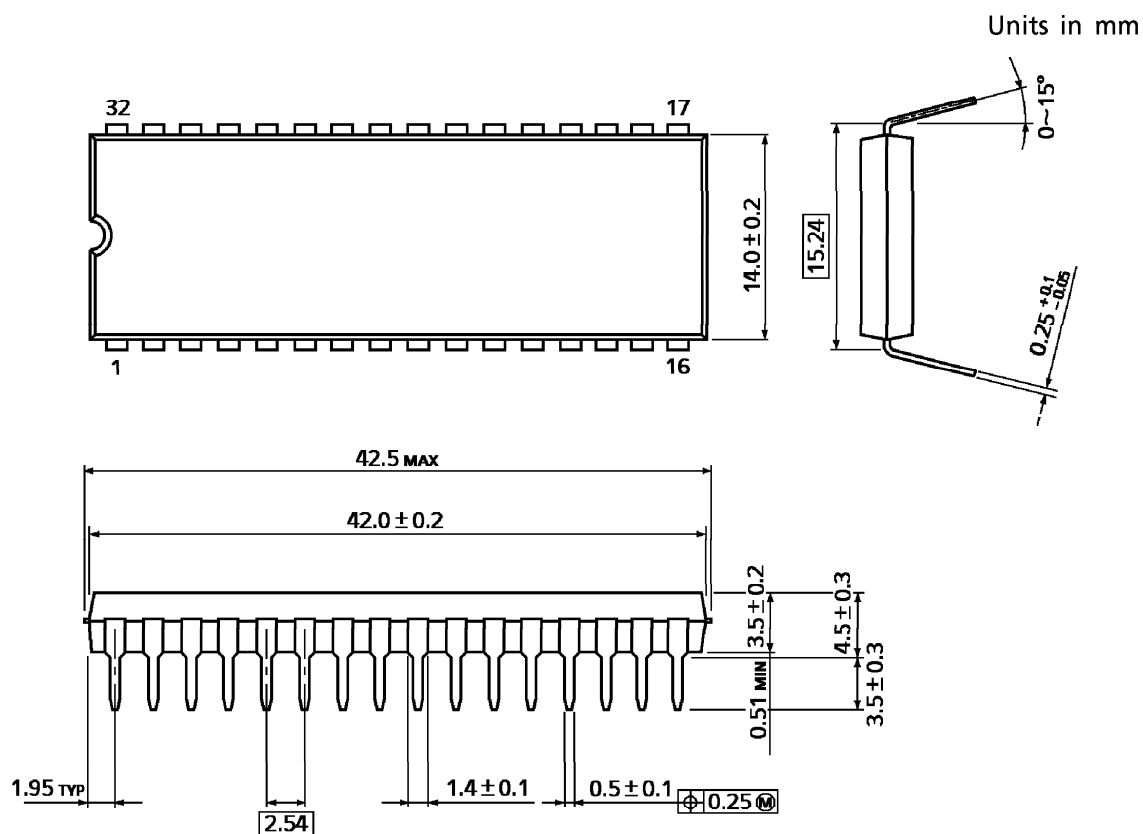


- Note: (1) In  $\overline{CE1}$  controlled data retention mode, minimum standby current mode is entered when  $CE2 \leq 0.2 \text{ V}$  or  $CE2 \geq V_{DD} - 0.2 \text{ V}$ .
- (2) When  $\overline{CE1}$  is operating at the  $V_{IH}$  level (2.2 V), the operation current is given by  $I_{DDSI}$  during the transition of  $V_{DD}$  from 4.5 to 2.4 V.
- (3) In  $CE2$  controlled data retention mode, minimum standby current mode is entered when  $CE2 \leq 0.2 \text{ V}$ .



# TOSHIBA TC551001CP/CF/CFT/CTR/CST/CSR-55,-70,-85,-55L,-70L,-85L

## PACKAGE DIMENSIONS (DIP32-P-600-2.54)

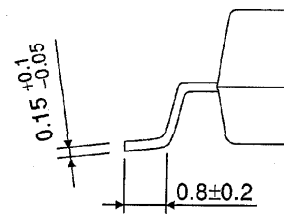
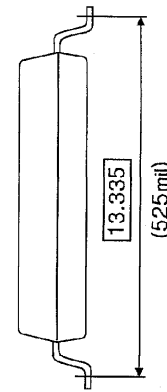
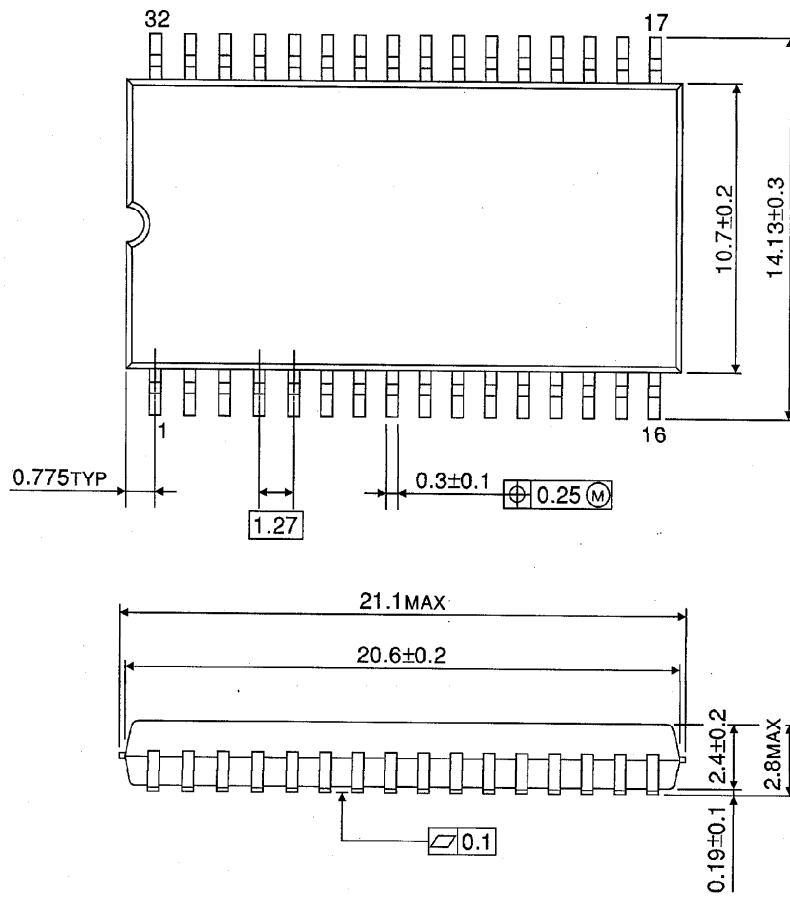


Weight: 4.45 g (typ)

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PACKAGE DIMENSIONS (SOP32-P-525-1.27)

Units in mm

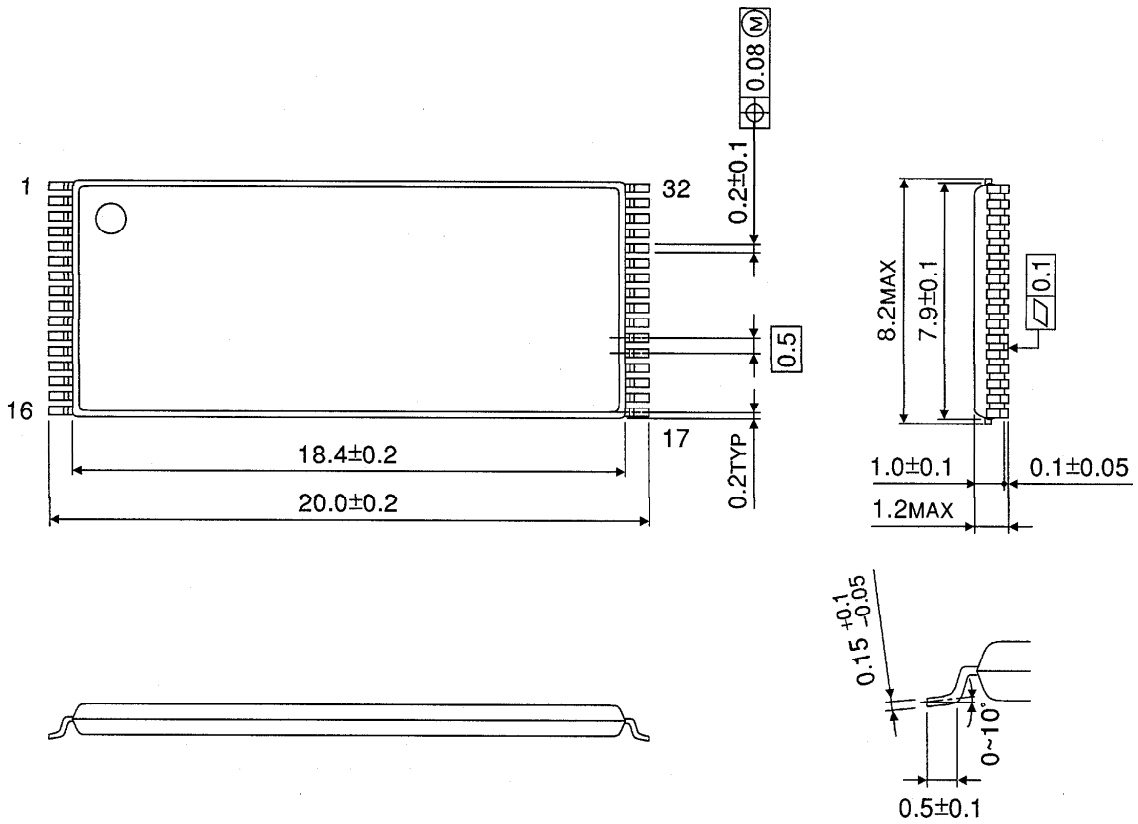


Weight: 1.04 g (typ)

# TOSHIBA TC551001CP/CF/CFT/CTR/CST/CSR-55,-70,-85,-55L,-70L,-85L

## PACKAGE DIMENSIONS (TSOP I 32-P-0820-0.50)

Units in mm

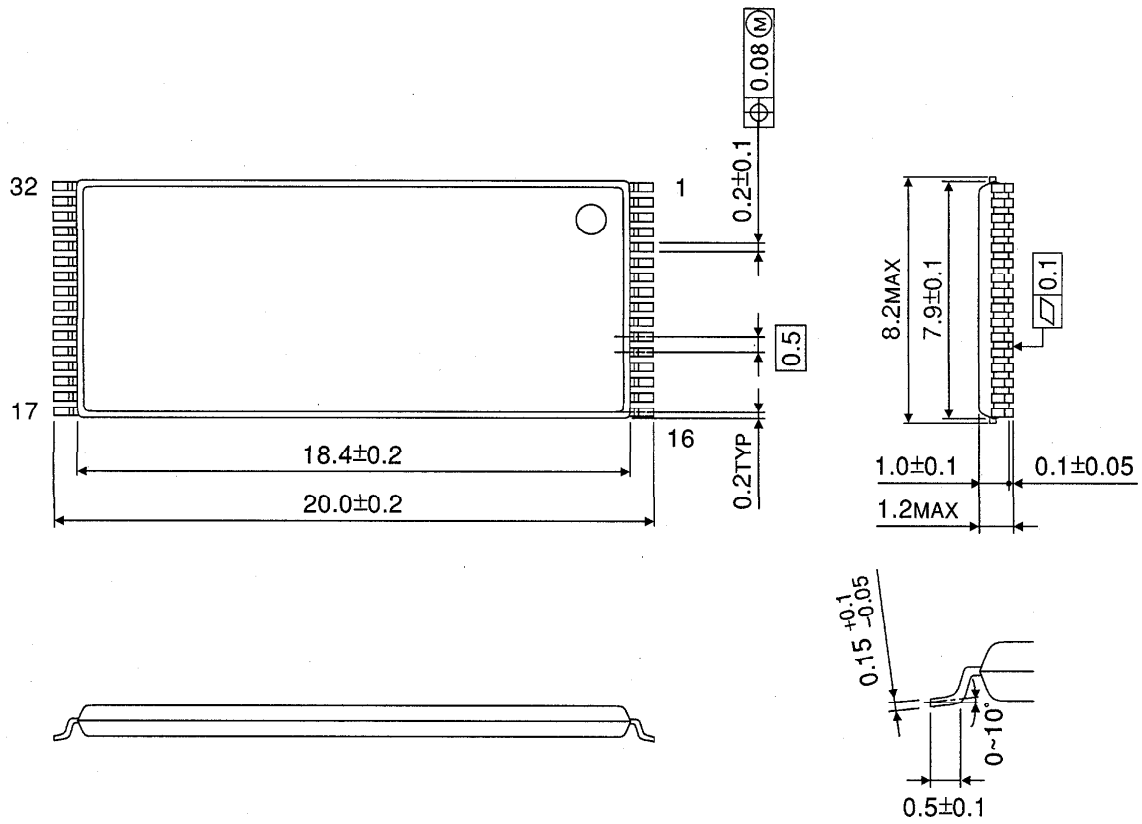


Weight: 0.34 g (typ)

# TOSHIBA TC551001CP/CF/CFT/CTR/CST/CSR-55,-70,-85,-55L,-70L,-85L

## PACKAGE DIMENSIONS (TSOP I 32-P-0820-0.50A)

Units in mm

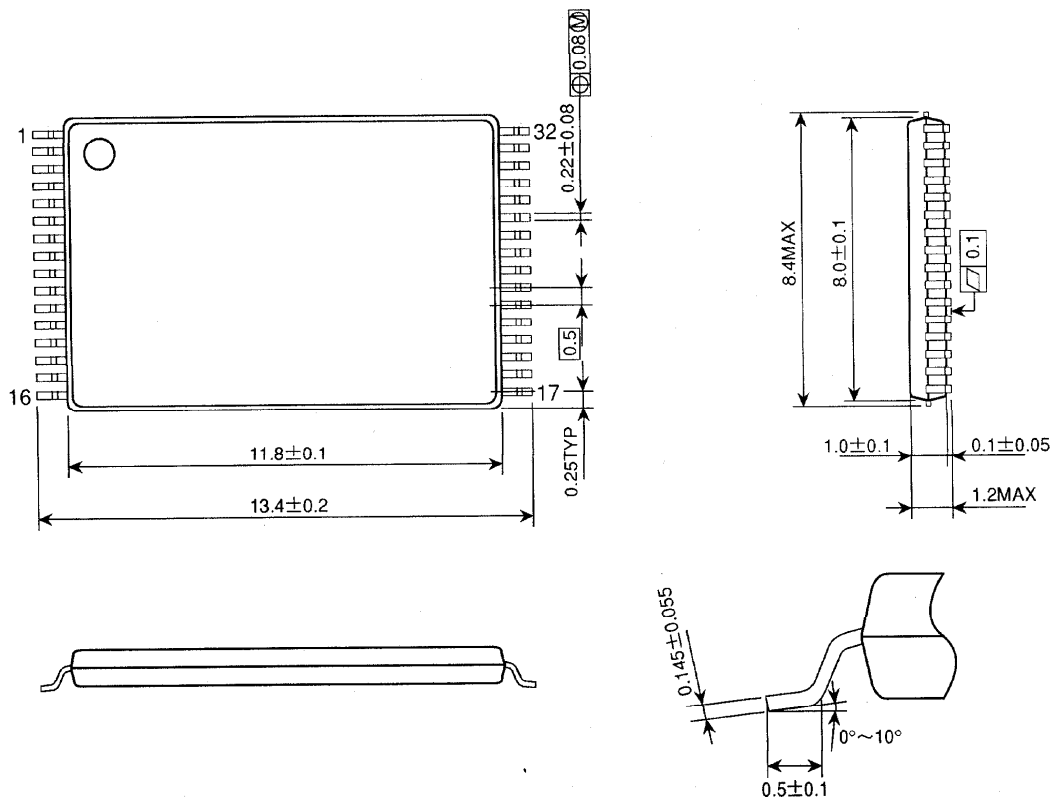


Weight: 0.34 g (typ)

# TOSHIBA TC551001CP/CF/CFT/CTR/CST/CSR-55,-70,-85,-55L,-70L,-85L

## PACKAGE DIMENSIONS (TSOP I 32-P-0.50)

Units in mm

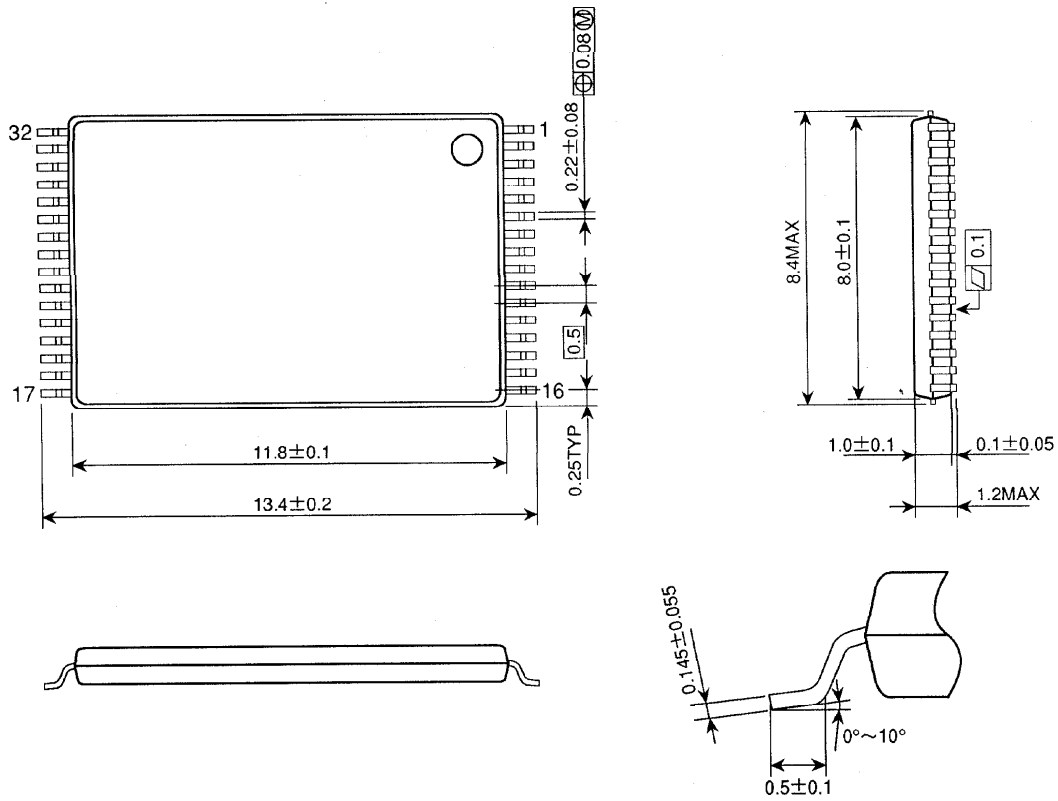


Weight: 0.24 g (typ)

# TOSHIBA TC551001CP/CF/CFT/CTR/CST/CSR-55,-70,-85,-55L,-70L,-85L

## PACKAGE DIMENSIONS (TSOP I 32-P-0.50A)

Units in mm



Weight: 0.24 g (typ)